



## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : YEH  
Application No. : 10/601,701  
Filed : June 24, 2002  
Title : METHOD FOR FABRICATION OF POLYCRYSTALLINE SILICON THIN FILM TRANSISTORS  
Group Art Unit : 2812  
Examiner : S. Isaac  
Docket No. : BHT/3230-56

*Please Enter S/17/05*  
Honorable Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**LETTER TO THE OFFICIAL DRAFTSPERSON**

Sir:

Enclosed are seven (7) sheets of new formal drawings (FIGS. 1-7) for the patent application noted above. Approval of the formal drawings is respectfully requested.

Respectfully submitted,

By:

  
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Reg. No. 26,592Date: March 3, 2005

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